PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-012746

(43)Date of publication of application : 16.01.1998

(51)Int.Cl. H01L 21/8238
H01L 27/092
H01L 27/04
H01L 21/822
H01L 29/78

(21)Application number : 08-164425

(22)Date of filing : 25.06.1996

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(54) SEMICONDUCTOR DEVICE

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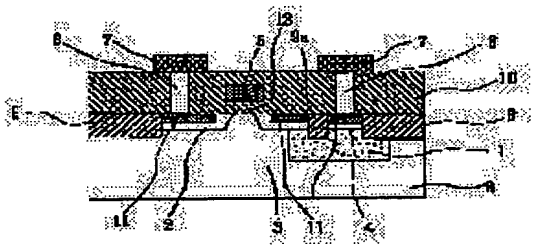
(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the thermal breakdown due to electrostatic pulses and improve the integration degree, by forming a lower concn. impurity diffused layer than a drain-source diffused layer of a MOS transistor between the drain- source diffused layer and the source-drain leading part.

SOLUTION: An N-channel MOS transistor gate electrode 5 is formed on a p-type Si substrate 8 through a gate insulation film 12, and an n-type source diffused layer 2 and an n-type drain diffused layer 3 are formed at both sides thereof. A high m.p. metal silicide layer 11 is formed on the surface thereof. Against thermal breakdown due to applied electrostatic pulses, an n-type low concn. impurity diffused layer 1 is formed between the diffused layer 3 formed through an element isolating insulation film 9a and a drain electrode leading n-type diffused layer 4. This improves the integration degree of an input/output protection circuit, without reducing the electrostatic breakdown resistance.



LEGAL STATUS

[Date of request for examination] 25.06.1996

[Date of sending the examiner's decision of rejection] 03.10.2000

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by having a gate electrode, having the source drain impurity diffused layer of this semi-conductor substrate and a reverse conductivity type on said semi-conductor substrate front face of the both sides of this gate electrode, and preparing one [at least] electrode fetch section of these source drain impurity diffused layer through a low-concentration impurity diffused layer with the same conductivity type as a source drain impurity diffused layer on a 1 conductivity-type semi-conductor substrate.
[Claim 2] The semiconductor device according to claim 1 with which the refractory metal silicide layer is formed in the front face of a source drain impurity diffused layer.
[Claim 3] The semiconductor device with which it is the CMOS mold semiconductor device which has an MOS mold semiconductor device according to claim 1 or 2, and the high impurity concentration and the conductivity type of the source drain impurity diffused layer of said MOS mold semiconductor device and the low-concentration impurity diffused layer arranged between the electrode fetch section are characterized by being the same as that of the high impurity concentration of the impurity diffused layer for substrate electrodes of said MOS mold semiconductor device and MOS mold semiconductor device of a reverse conductivity type, and a conductivity type respectively.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the semiconductor device containing the MOS transistor and this transistor which have improved electrostatic-discharge resistance about a semiconductor device.
[0002]
[Description of the Prior Art] An advance of the ultra-fine processing technology in recent years in manufacture of semiconductor integrated circuit equipment is remarkable. Especially the advance of the detailed-ized technique of an MOS transistor is remarkable, and is acting to the so-called deep submicron age of 0.5 micrometers or less of channel length as ** people in current advanced technology.
[0003] The technique which forms a refractory metal silicide layer in the front face of the impurity diffused layer which forms a source drain for reduction of the parasitism resistance accompanying detailed-izing with the semiconductor integrated circuit equipment containing the detailed MOS transistor below submicron one is in use. By forming a refractory metal silicide layer, the sheet resistance of a source drain can be reduced from 100ohms / ** extent to below 10ohms / ** extent. Since the switching speed of an MOS transistor can be raised by reducing parasitism resistance, the actual condition is that the refractory metal silicide layer is utilized positively.
[0004] However, reducing parasitism resistance of a source drain brings about the evil in which the resistance (static electricity destructive resistance) is reduced on the contrary, in the MOS transistor which is arranged at the I/O section of semiconductor integrated circuit equipment, and is used for the static electricity protection against destruction from the outside. The cause that this resistance falls is that parasitism resistance decreases, it serves as a big value, flows the MOS transistor section, without controlling the discharge current when the static electricity pulse is added, and is for a thermal runaway to arise.
[0005] Hereafter, the solution means by the cause and the conventional technique which this thermal runaway produces is explained using a drawing. A circuit diagram when drawing 3 uses an N-channel metal oxide semiconductor transistor for electrostatic protection at the input section, the layout top view of an N-channel metal oxide semiconductor transistor having shown the solution means according [drawing 4 (a)] to the conventional technique, and drawing 4 (b) are the B-B line sectional views of drawing 4 (a). In addition, drawing 4 (a) is omitting the substrate etc.
[0006] First, the cause which a thermal runaway produces by the static electricity pulse is explained using drawing 3 and drawing 4 . In drawing 3 , the gate electrode, source electrode, and substrate electrode of an N-channel metal oxide semiconductor transistor (23) are connected to an earth terminal (24), and the drain electrode is connected to the input terminal (21). An NPN parasitism bipolar transistor (25) is a lateral NPN bipolar transistor parasitically constituted with the N type impurity diffused layer which forms the source electrode and drain electrode of an N-channel metal oxide semiconductor transistor (23), and a P type substrate electrode.
[0007] In the state of anticipated use, an N-channel metal oxide semiconductor transistor (23) is an

OFF state, and the signal inputted into input **** (21) is spread to an output terminal (22) as it is, and is further spread by it to the internal circuitry of the point. When the static electricity pulse of negative polarity is impressed to an input terminal (21) to an earth terminal (24), forward bias of the N type drain electrode of an N-channel metal oxide semiconductor transistor (23) and the PN-junction diode formed by P type substrate inter-electrode is carried out, it discharges, and, thereby, an internal circuitry is protected. In that case, since forward current only flows to the PN-junction diode to which discharge takes place, there is little potential difference and calorific value also has it, it is rare for lowering of the static electricity resistance by the thermal runaway to become a problem. [little] On the other hand, when the static electricity pulse of a positive electrode is added to an earth terminal (24), the reverse bias of the PN-junction diode first formed between the N type drain electrode (collector) of an N-channel metal oxide semiconductor transistor (23) and a P type substrate electrode (base) is carried out, and breakdown arises. If this breakdown current flows, forward bias of the PN junction between earth terminals (emitter) will be carried out to a P type substrate electrode (base) for parasitism resistance of a P type silicon substrate, and an NPN parasitism bipolar transistor (25) will carry out a turn-on. The static electricity pulse impressed to the input terminal (21) because an NPN parasitism bipolar transistor carries out a turn-on discharges to an earth terminal (24), and the internal circuitry is protected.

[0008] Actuation of an NPN parasitism bipolar transistor poses a problem here. Generally the bipolar transistor of an ON state has the property that collector current increases, with the temperature rise, if the discharge current becomes large, a temperature rise will happen and a current will further become easy to flow. That is, it means that positive feedback had started, a thermal run away is carried out as a result, and it results in a thermal runaway. The thermal runaway by the thermal run away of such a parasitism bipolar transistor is the problem which did not surface since the collector current of an NPN parasitism bipolar transistor was controlled by parasitism resistance without the refractory metal silicide layer by the time of 1 micrometers or more of channel length when parasitism resistance was comparatively strong.

[0009] How to raise the static electricity resistance by devising the number of resistance sheets and layout pattern of a source-drain region, and making parasitism resistance increase intentionally conventionally as a means to solve such a problem was considered (for example, JP,6-84941,A).

[0010] Drawing 4 (a) is the layout top view of an N-channel metal oxide semiconductor transistor showing an example of the conventional technique, and drawing 4 (b) is the B-B line sectional view of drawing 4 (a). An N-channel metal oxide semiconductor transistor gate electrode (5) is formed through gate dielectric film (12) on a P type silicon substrate (8), with the P type silicon substrate, the N type source diffusion layer (2) and N type drain diffusion layer (3) of a reverse conductivity type are arranged in the both sides, and the refractory metal silicide layer (11) is formed in the front face, respectively. A source drain electrode is connected outside through an embedded contact hole (6) and metal wiring (7). The insulation with other MOS transistors is performed by the insulator layer for isolation (9), and the insulation during metal wiring is performed by the insulator layer between wiring layers (10). In order to cope with the thermal runaway at the time of the static electricity pulse impression, the neck field (31) as shown in drawing 4 (a) is prepared. The excessive discharge current to the N-channel metal oxide semiconductor transistor section is controlled by buildup of the resistance by this neck field.

[0011]

[Problem(s) to be Solved by the Invention] However, in the above-mentioned Prior art, in order to increase the resistance of a source-drain region required to prevent the thermal runaway by the static electricity pulse, a big area was needed and there was a problem that a degree of integration fell. This has the low sheet resistance of the neck field of a source-drain region, and for acquiring desired resistance, it is because [making it long] it can kick, and there is nothing if it is ** about a neck field.

[0012] Then, the object of this invention is offering the semiconductor integrated circuit equipment which the thermal runaway by the static electricity pulse is prevented (electrostatic-discharge resistance's improved), and contains the high semiconductor device and this semiconductor device of a

degree of integration.
[0013]
[Means for Solving the Problem] this invention person completed this invention, as a result of repeating various examination, in order to attain the above-mentioned object.
[0014] The 1st invention has a gate electrode on a 1 conductivity-type semi-conductor substrate, has the source drain impurity diffused layer of this semi-conductor substrate and a reverse conductivity type on said semi-conductor substrate front face of the both sides of this gate electrode, and relates to the semiconductor device characterized by preparing one [at least] electrode fetch section of these source drain impurity diffused layer through a low-concentration impurity diffused layer with the same conductivity type as a source drain impurity diffused layer.
[0015] The 2nd invention relates to the semiconductor device of the 1st invention with which the refractory metal silicide layer is formed in the front face of a source drain impurity diffused layer.
[0016] The 3rd invention is a CMOS mold semiconductor device which has the 1st or the MOS mold semiconductor device of the 2nd invention, and relates to the semiconductor device with which the high impurity concentration and the conductivity type of the source drain impurity diffused layer of said MOS mold semiconductor device and the low-concentration impurity diffused layer arranged between the electrode fetch section are characterized by being the same as that of the high impurity concentration of the impurity diffused layer for substrate electrodes of said MOS mold semiconductor device and MOS mold semiconductor device of a reverse conductivity type, and a conductivity type respectively.
[0017]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained using a drawing.
[0018] Operation gestalt 1 drawing 1 (a) is the layout top view of the N-channel metal oxide semiconductor transistor which is 1 operation gestalt of the semiconductor device of this invention, and drawing 1 (b) is the A-A line sectional view of drawing 1 (a). In addition, drawing 1 (a) is omitting the substrate etc. An N-channel metal oxide semiconductor transistor gate electrode (5) is formed through gate dielectric film (12) on a P type silicon substrate (8), with the P type silicon substrate, the N type source diffusion layer (2) and N type drain diffusion layer (3) of a reverse conductivity type are arranged in the both sides, and the refractory metal silicide layer (11) is formed in the front face, respectively. A source drain electrode is connected outside through an embedded contact hole (6) and metal wiring (7). The insulation with other MOS transistors is performed by the insulator layer for isolation (9), and the insulation during metal wiring is performed by the insulator layer between wiring layers (10). In order to cope with ****** at the time of the static electricity pulse impression, the N type low concentration impurity diffused layer (1) is prepared between the N type drain diffusion layer (3) currently formed through the insulator layer for isolation (9a), and the N type diffusion layer for drain electrode fetch (4).
[0019] Next, the case where it is used for the input-protection circuit which shows the N-channel metal oxide semiconductor transistor which showed actuation of this operation gestalt to drawing 1 to drawing 3 is explained. First, if the static electricity pulse of a negative electrode is impressed to an input terminal (21) to an earth terminal (24), forward bias of the PN-junction diode constituted by a P type silicon substrate (8), an N type low concentration impurity diffused layer (1), and the N type drain diffusion layer (3) will be carried out, it will discharge, and an internal circuitry will be protected. On the other hand, when the static electricity pulse of a positive electrode joins an input terminal to an earth terminal, the reverse bias of the PN-junction diode first formed between the N type drain electrode (collector) of an N-channel metal oxide semiconductor transistor and a P type substrate electrode (base) is carried out, and breakdown arises. If this breakdown current flows, forward bias of the PN junction between earth terminals (emitter) will be carried out to a P type substrate electrode (base), and an NPN parasitism bipolar transistor (25) will carry out a turn-on to the parasitism ****** sake of a P type silicon substrate. The static electricity pulse impressed to the input terminal because this NPN parasitism bipolar transistor carries out a turn-on discharges to an earth terminal, and an internal

circuitry is protected. In that case, since an electrostatic-discharge current flows through an N type low concentration impurity diffused layer (1) as shown in drawing 1 (b), it can prevent the thermal run away of a parasitism NPN bipolar transistor, and a thermal runaway does not produce it. Since the resistance of the drain section is increased by preparing an N type low concentration impurity diffused layer, prevention of a thermal runaway can be performed in a very small area. Also in the case of the P channel MOS transistor which completely carried out the conductivity type reversely, the same effectiveness is demonstrated although the example of an N-channel metal oxide semiconductor transistor was explained here.

[0020] The operation gestalt 2, next the 2nd operation gestalt of this invention are explained using drawing 2 . Drawing 2 is the sectional view of an example which applied this invention to the CMOS mold semiconductor device. The N-channel metal oxide semiconductor transistor gate electrode (5) is formed through gate dielectric film (12) on the P type silicon substrate (8). On the N type well (15) field, the P channel MOS transistor gate electrode (16) is formed through gate dielectric film (12). With the P type silicon substrate, the N type source diffusion layer (2) and N type drain diffusion layer (3) of a reverse conductivity type are arranged in the both sides of an N-channel metal oxide semiconductor transistor gate electrode (5), and the refractory metal silicide layer (11) is formed in the top face. with an N type well, the P type source diffusion layer (13) and P type drain diffusion layer (14) of a reverse conductivity type arrange in the both sides of a P channel MOS transistor gate electrode (16) — having — **** — the front face — a refractory metal silicide layer (11) — each is formed. A source drain electrode is an embedded contact hole (6) and metal wiring (it connects with the exterior through 70.). The insulation with other MOS transistors is performed by the insulator layer for isolation (9), and the insulation during metal wiring is performed by the insulator layer between wiring layers (10).

[0021] The description of this operation gestalt is the high impurity concentration as the N type well (15) which constitutes a P channel MOS transistor with the same high impurity concentration of an N type low concentration impurity diffused layer (1) besides the description of the operation gestalt 1. That is, in the CMOS mold semiconductor device using a P type silicon substrate, while forming an indispensable N type well (impurity diffused layer for substrate electrodes), an N type low concentration impurity diffused layer can be formed. Therefore, a desired semiconductor device can be manufactured, without making a production process increase.

[0022] Although this operation gestalt showed the example of the CMOS mold semiconductor integrated circuit equipment which used the P type silicon substrate, it is possible similarly to form a P type low concentration impurity diffused layer between the source drain diffusion layer of a P channel MOS transistor and the source drain electrode fetch section at the same time it forms a P type well using an N type silicon substrate.

[0023] Furthermore, when forming both a P channel MOS transistor and an N-channel metal oxide semiconductor transistor on a well field, a low concentration impurity diffused layer can be formed at formation and coincidence of a well between the source drain diffusion layer of both MOS transistors, and the source drain electrode fetch section, and a desired semiconductor device can be produced, without increasing a production process.

[0024]

[Example] The above-mentioned concrete numeric value and above-mentioned ingredient of the operation gestalt 1 are explained, and the effectiveness in that case is explained further.

[0025] the channel length of a gate electrode — 0.25 micrometers and gate dielectric film — in the high impurity concentration of 1x1017 atom/cm3, an N type source diffusion layer, an N type drain diffusion layer, and the N type diffusion layer for drain electrode fetch, the high impurity concentration of 1x1020 atom/cm3 and an N type low concentration impurity diffused layer constituted [the high impurity concentration of silicon oxide of 60A of thickness, and a P type silicon substrate] the MOS transistor from a substrate front face as a depth of 1 micrometer by 1x1017 atom/cm3. The alloy of aluminum and Cu was adopted as metal wiring, W was embedded at the embedding contact hole and the titanium

silicide layer was adopted as a refractory metal silicide layer.
[0026] Actuation when the static electricity pulse is impressed is as the above-mentioned operation gestalt 1 having explained. The sheet resistance of an N type low concentration impurity diffused layer was about 500ohms. Moreover, even when eight-piece parallel connection of the N-channel metal oxide semiconductor transistor with a channel width of 40 micrometers which formed spacing of a gate electrode edge and an embedded contact hole edge by only 2.4 micrometers was carried out as a result of carrying out the static electricity breakdown test according to MIL-STD -883, and an input-protection circuit was constituted, the resistance beyond 3000V was able to be maintained.
[0027]
[Effect of the Invention] The 1st effectiveness of this invention is being able to improve the degree of integration of the I/O protection network section, without reducing static electricity destructive resistance. This is because resistance are arranging a low-concentration impurity diffused layer, and required for prevention of the thermal runaway by the static electricity pulse is realizable in small area from a source drain diffusion layer between the source drain diffusion layer of an MOS transistor, and the source drain electrode fetch section.
[0028] The 2nd effectiveness of this invention is that desired equipment is producible, without increasing a production process, when this invention is applied to a CMOS mold semiconductor device. This is because the source drain diffusion layer of a 1 conductivity-type MOS transistor (for example, N-channel MOS transistor) and the low-concentration impurity diffused layer arranged between the source drain electrode fetch sections can be formed in formation and coincidence of the substrate electrode of a reverse conductivity-type MOS transistor (for example, P-channel MOS transistor).

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the explanatory view of the semiconductor device of this invention.
[Drawing 2] It is the explanatory view of the semiconductor device of this invention.
[Drawing 3] It is a circuit diagram at the time of applying this invention or the conventional semiconductor device to the input section for electrostatic protection.
[Drawing 4] It is the explanatory view of the conventional semiconductor device.
[Description of Notations]
1 N Type Low Concentration Impurity Diffused Layer
2 N Type Source Diffusion Layer
3 N Type Drain Diffusion Layer
4 N Type Drain Diffusion Layer for Electrode Fetch
5 N-channel Metal Oxide Semiconductor Transistor Gate Electrode
6 Embedded Contact Hole
7 Metal Wiring
8 P Type Silicon Substrate
9 9a Insulator layer for isolation
10 Insulator Layer between Wiring Layers
11 Refractory Metal Silicide Layer
12 Gate Dielectric Film
13 P Type Source Diffusion Layer
14 P Type Drain Diffusion Layer
15 N Type Well
16 P Channel MOS Transistor Gate Electrode
21 Input Terminal
22 Output Terminal
23 N-channel Metal Oxide Semiconductor Transistor
24 Earth Terminal
25 NPN Parasitism Bipolar Transistor
31 Neck Field

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